**In The Abstract**

Please substitute Abstract as follows:

[0028] A programmable memory controller having a main memory device, a command decoder, a ~~cycle~~period setting device, a command-sequencing device and a command signal output device. When the programmable memory controller needs to access data inside a memory unit, the memory controller sends out a request signal. The command decoder receives the request signal and decodes the request signal to produce ~~a plurality of~~ command signals. The ~~cycle~~period setting device receives a control signal and decodes the control signal to produce a ~~cycle~~period setting signal. The control signal controls the maintenance period of the command signals. The command-sequencing device receives the command signals and the ~~cycle~~period setting signals to sequence the command signals. The command signal output device receives the sequenced command signals and the ~~cycle~~period setting signal so that the sequenced command signal is sent to the memory unit during the maintenance period according to indications provided by the ~~cycle~~period setting signals.